

CAPACITIVELY COUPLED CHIP-TO-CHIP INTERCONNECT DESIGN



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CAPACITIVELY COUPLED CHIP-TO-CHIP INTERCONNECT DESIGN

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Condition: New. Publisher/Verlag: VDM Verlag Dr. Müller | A low-power high-bandwidth I/O solution for future high performance VLSI chips | I/O bandwidth in the Multi-Tb/s range is required for current and future high performance VLSI chips. This trend demands high-speed, high-density and low power I/Os. AC coupled interconnect (ACCI) has been demonstrated as a systematic solution for providing higher pin density and lower power dissipation. ACCI utilizes non-contact capacitor plates as signal I/O which yields a much higher pin density than traditional solder bump I/O. ACCI saves significant power with pulse signaling. A test-chip with a complete capacitively coupled serial link is designed including: multi-phase DLL, serializer, transmitter, pulse receiver, clock and data recovery and deserializer. A 3Gb/s ACCI chip-to-chip communication is demonstrated through two 150fF coupling capacitors and a 15 cm microstrip line. A fully differential pulse receiver design is also demonstrated with 6-bit bus running at an aggregate bandwidth of 36Gb/s. Signal integrity issues associated with the ACCI bus, such as crosstalk and switching noise, are discussed. Simulation results demonstrate that higher data rates over ACCI channels can be achieved with more advanced CMOS technologies. | Format: Paperback | Language/Sprache: english | 140 pp.

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