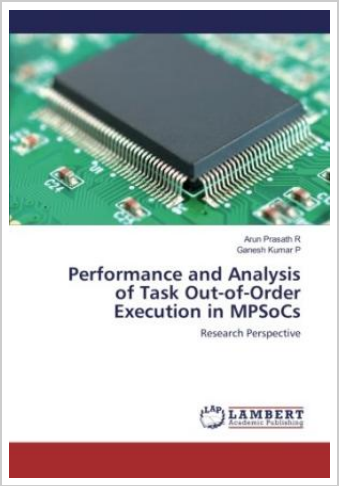

Performance and Analysis of Task Out-of-Order Execution in MPSoCs

By Prasath R, Arun / Kumar P, Ganesh

Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | Research Perspective | The inter-subsystem communication structure can be optimized at the beginning of the design process by using simulation models at three different abstraction levels. Some design loop cases can be avoided by using this exploration method. With the Motion-JPEG case study, and illustrate the whole communication exploration process step by step. From experimental results, it show that compared with the cycle accurate simulation, the inter subsystem communication can be well optimized and evaluated at higher abstraction levels. In this project, a solution for a classification problem that is used for optimized packet assignment to different data paths within a network processor System-on-Chip (SoC). Based on a specification of the usage case for our classifier it derive Heterogeneous Decision Graph Algorithm (HDGA), a heuristic approach to construct a decision tree classifier that integrates external lookup results for certain types of rules. Evaluated various parameters for optimizing the proposed decision tree and present simulation results to show the scalability of HDGA for typical problem sizes. This project is concluded with the results of an implementation on our FPGA Platform. | Format: Paperback | Language/Sprache: english | 76 pp.

Reviews

This ebook is really gripping and fascinating. it had been writtern extremely perfectly and useful. Once you begin to read the book, it is extremely difficult to leave it before concluding.

-- ***Leopold Hills***

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