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UDSM CMOS CIRCUITS

Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | Delay & Power Models | A simple and accurate delay model is proposed for Ultra Deep Sub-micron CMOS circuits (CMOS Inverter, NAND2, NOR2 etc) based on nth power law when the channel length is less than the 90nm. All the parameters are taken from BSIM.4.6.1 manual. This work derives analytical expression for the delay model of a CMOS inverter including all sorts of secondary effects i.e. Body Bias effect, Channel Length Modulation...

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