



## Timing Optimization Through Clock Skew Scheduling

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By Ivan S. Kourtev

Springer-Verlag GmbH Nov 2008, 2008. Buch. Condition: Neu. Neuware - The focus of this book is on timing analysis and optimization techniques for circuits with level-sensitive memory elements (registers). Level-sensitive registers are becoming significantly more popular in practice as integrated circuit densities are increasing and the performance-per-power metric for integrated circuits becomes a key issue. Therefore, techniques for understanding level-sensitive based circuits and for optimizing the performance of such circuits are increasingly important. The book includes the following major topics in the timing analysis and optimization of level-sensitive circuits: A linear programming (LP) formulation applicable to the timing analysis of large scale circuits. The formulation uses a variation of the big M method - called the modified big M method - to transform the non-linear constraints in the problem formulation into solvable linear constraints. This LP formulation is computationally efficient and demonstrates significant circuit performance improvement. By making maximum use of cycle stealing, operation at a higher clock frequency (reduced clock period) is possible. A delay insertion methodology that improves the efficiency of clock skew scheduling in level-sensitive circuits. It is shown that re-convergent paths limit the improvement of circuit performance that can be achieved through clock skew scheduling. The...



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