

Interconnect Technology for Three-Dimensional Chip Integration



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INTERCONNECT TECHNOLOGY FOR THREE-DIMENSIONAL CHIP INTEGRATION

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Cuvillier Verlag Okt 2007, 2007. Taschenbuch. Condition: Neu. Neuware - 3D-integration, or vertical chip integration, is a technology that aims to shorten the interconnect path between integrated circuits and to increase the interconnect density by using through-chip micro vias. It allows a smaller circuit footprint by chip-stacking and can combine a variety of technologies. This thesis treats the technological aspects of a novel 3D-integration concept, which is based on processes that follow the sequence: wafer thinning, via processing, chip stacking. The micro vias are processed from the backside and therefore do not impose routing restrictions on the front side of the circuit. As an example application, the two key elements, the micro vias and the micro joints are formed on bare silicon substrate. It is shown how an electrical interconnect path from the top to the bottom of a mechanically sound chip stack can be realized. The process of stacking employs a solder based bonding method, which results in a rigid and thermally stable connection. By solid-liquid interdiffusion (isothermal solidification) the solder filled connection zone is entirely transformed into intermetallic compounds. This results in a homogenized and rigid joint with excellent mechanical properties, suitable for step by step stack building. Further, the scaling of microjoints in such 3-dimensional chip-stacks is proposed by means of kinetic control. Therefore, phase growth in the copper-tin system in the presence of various metal barriers at the interface is evaluated. Promising results have been obtained by using layers of Ti, Ta, Ti:W or combilayers thereof in a thickness range of 20 to 50 nm. These results suggest a miniaturization potential of solder based microjoints down to the scale of 1 μm , along with the respective increase in interconnect density. 117 pp. Englisch.

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